CLAIMS

1. A method for changing a clock frequency in a system (10) comprising a plurality of synchronous integrated circuit chips (12, 14, 16), comprising:

detecting a change in processing requirements in one of the plurality of synchronous integrated circuit chips;

notifying the plurality of synchronous integrated circuit chips that a clock frequency change is to occur;

achieving a quiescent bus state in each of the plurality of synchronous integrated circuit chips;

notifying the plurality of synchronous integrated circuit chips that the clock frequency change may occur; and

changing the clock frequency of the plurality of integrated circuit chips.

2. The method of claim 1, wherein the clock frequency comprises at least one of a processor clock frequency and a bus clock frequency.

3. The method of claim 1, wherein changing the clock frequency of the plurality of integrated circuit chips comprises, for each integrated circuit chip:

stopping a bus clock of the integrated circuit chip;

changing the clock frequency of the integrated circuit chip; and

restarting the bus clock of the integrated circuit chip.

4. The method of claim 3, wherein changing the clock frequency of the integrated circuit chip results in a change in a clock frequency of the bus clock, and wherein a ratio of the clock frequency of the integrated circuit chip to the clock frequency of the bus clock remains constant.

5. The method of claim 1, wherein changing the clock frequency of the integrated circuit chip comprises:

determining a new clock frequency;

selecting a divider value for adjusting an existing clock frequency; and

applying the divider value to the existing clock frequency to obtain the new clock frequency.

6. The method of claim 1, wherein notifying the plurality of synchronous integrated circuit chips that the clock frequency change may occur takes place only after all of the plurality of synchronous integrated circuit chips have achieved a quiescent bus state.

7. The method of claim 1, wherein the plurality of synchronous integrated circuit chips (12, 14, 16) comprises a plurality of processors (12, 14) and a companion chip (16), and wherein:

the companion chip (16) receives a control transaction requesting the clock frequency change from the processor (12, 14) in which the change in processing requirements was detected; and

the companion chip (16) broadcasts the control transaction to the plurality of processors (12, 14).

8. The method of claim 7, wherein the companion chip (16) broadcasts the control transaction over a bus (18) that interconnects the companion chip (16) and the plurality of processors (12, 14), and wherein the plurality of processors (12, 14) obtain the control transaction by snooping the bus (18).

9. The method of claim 7, wherein, after being notified that a clock frequency change is to occur, each of the plurality of processors (12, 14) achieves a quiescent bus state and sends an acknowledgement to the companion chip (16).

10. The method of claim 9, wherein, after receiving the acknowledgement from all of the plurality of processors (12, 14), the companion chip (16) notifies the plurality of processors (12, 14) that the clock frequency change may occur.

11. The method of claim 10, wherein the plurality of processors (12, 14) perform a frequency change operation.

12. The method of claim 11, wherein the companion chip (16) performs a frequency change operation after the frequency change operation has been completed by the plurality of processors (12, 14).

13. The method of claim 9, wherein, after receiving the acknowledgement from all of the plurality of processors (12, 14), the companion chip (16) achieves a quiescent bus state, turns off its bus clock, and notifies the plurality of processors (12, 14) that the clock frequency change may occur.

14. An apparatus for changing a clock frequency, comprising:

a phase-lock-loop circuit (20) for providing a constant frequency signal in synchronism with a reference clock signal, wherein the constant frequency signal has a frequency f;

a plurality of divider circuits (28) receiving the constant frequency output signal from the phase-lock-loop circuit (20), each divider circuit providing an output signal having a frequency given by f/d_n and synchronous with the constant frequency signal of the phase-lock-loop circuit (20), wherein d_n is a divider value of an nth divider circuit (28); and

a multiplexer (30) for receiving the output signals from the plurality of divider circuits (28) and for selecting, based on a frequency selection signal, the output signal from one of the plurality of divider circuits (28), having a desired frequency, to serve as a processor clock signal (pclk).

15. The apparatus of claim 14, wherein the processor clock frequency is changed by selecting the output signal of a different one of the plurality of divider circuits (28) to serve as the processor clock signal (pclk).

16. The apparatus of claim 14, further comprising a bus divider circuit (32) for receiving the processor clock signal and for outputting a bus clock signal (bclk) in synchronism with the processor clock signal (pclk), wherein bclk is given by pclk/b, and wherein b is a divider value of the bus divider circuit (32).

17. The apparatus of claim 16, wherein a ratio of the frequency of the processor clock signal (pclk) to the frequency of the bus clock signal (bclk) remains constant.

18. The apparatus of claim 14, wherein the phase-lock-loop circuit (20) comprises a PLL (22) and a feedback divider (24), and wherein the reference clock and an output of the feedback divider (24) are input into the PLL (22).

19. A method for changing processor and bus clock frequencies in a system (10) comprising a plurality of synchronous processors (12, 14), comprising:

detecting a change in processing requirements in one of the plurality of processors;

notifying the plurality of processors that processor and bus clock frequency changes are to occur;

achieving a quiescent bus state in each of the plurality of processors;

notifying the plurality of processors that the processor and bus clock frequency changes may occur; and

changing the processor and bus clock frequencies of each of the plurality of processors.

20. The method of claim 19, wherein a ratio of the processor clock frequency and the bus clock frequency of each processor (12, 14) remains constant.